Mattia Vezzoli

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Education

Yale University, New Haven, CT — Sept 2022 – May 2027
PhD Candidate in Electrical and Computer Engineering
Asynchronous VLSI and Architecture Lab (AVLSI). Advisor: Prof. Rajit Manohar

Yale University, New Haven, CT — Sept 2020 – Sept 2022
M.S. and M.Phil. in Electrical Engineering

Università degli Studi di Brescia, Brescia, Italy — Sept 2011 – Sept 2019
M.S. and B.S. in Electrical Engineering

Technical Skills

Programming: System Verilog, Verilog, Python, ACT (Asynchronous Circuit Toolkit), MATLAB, LabVIEW, MVTech HALCON.

Tools: Vivado, Virtuoso, ACT, Magic VLSI, Xyce, LabVIEW, GitHub, OpenCV.

Expertise: ASIC, VLSI, and RTL design, implementation, and verification; low-power deep learning accelerator design; FPGA; synchronous and asynchronous circuit design; computer architecture; machine learning; convolutional neural networks (CNNs); deep learning; vision systems; silicon photonics.

Research and Work Experience

Yale University, Ph.D. Candidate in Electrical and Computer Engineering — Sept 2022 – Present

- Developing the first fully asynchronous, low-power, and low-latency ASIC for convolutional neural network acceleration. ASIC architecture optimized for edge AI applications, supporting quantized integer-only computation and unstructured sparse workloads.
- Conducting detailed power and energy analyses by mapping the accelerator design into multiple synchronous and asynchronous circuit families to quantify efficiency trade-offs.
- Validating the chip through end-to-end CNN model execution, achieving near–floating-point accuracy using quantized integer-only arithmetic.

Lawrence Livermore National Lab Graduate Student Intern, Livermore, CA — May 2024 – Aug 2024

- Worked on the development of the first fully asynchronous, low-power, and low-latency ASIC for convolutional neural network acceleration. ASIC architecture optimized for edge AI applications, supporting integer-only computation and unstructured sparse workloads.

Yale University, M.S. in Electrical and Computer Engineering — Sept 2020 – Sept 2022

- Contributed to the development of the first photonic integrated circuit (PIC) titanium:sapphire laser.
- Modeled and simulated silicon photonic devices; performed cleanroom fabrication, testing, and device characterization.

Antares Vision, Software Engineer, R&D Department, Brescia, Italy — Oct 2018 – Nov 2020

- Designed and prototyped custom vision systems solutions for industrial quality control, defect detection and production line monitoring. Planned camera and illumination setup, defined technical requirements of the system.
- Developed image processing algorithms for object fault detection.
- System integration, troubleshooting, and electrical cabling of industrial machines.

Universita' degli studi di Brescia, MS in Electrical Engineering — Sept 2016 – Sept 2018

- Final Thesis project: FPGA based active stabilization of an interferometer at an arbitrary phase and verification of time-energy entanglement in a photon pair using long delay.

Universita' degli studi di Brescia, BS in Electrical Engineering Sept 2011 – May 2016

– Final Thesis project: Machine learning based automatic segmentation of irises and pupils in digital images.

Publications

- Vezzoli, M., Nel, L., Bhardwaj, K., Manohar, R., and Gokhale, M. (2024, March). Designing an Energy-Efficient Fully-Asynchronous Deep Learning Convolution Engine. In *2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)* (pp. 1–2). IEEE.
- Wang, Y., Holguín-Lerma, J.A., Vezzoli, M., Guo, Y., and Tang, H.X. (2023). Photonic-circuit-integrated titanium: sapphire laser. *Nature Photonics*, 17(4), pp. 338–345.
- Holguín-Lerma, J.A., Wang, Y., Guo, Y., Vezzoli, M., and Tang, H.X. (2022, October). Narrow-linewidth GaN lasers based on an AlN photonic integrated circuit. In *Frontiers in Optics* (pp. FM1E–2). Optica Publishing Group.
- Wang, Y., Guo, Y., Holguín-Lerma, J.A., Vezzoli, M., and Tang, H.X. (2024). Wafer-Scale Fabrication of a Titanium-Sapphire Laser Substrate by Thermal Diffusion. *ACS Photonics*, **11**(8), pp. 3303–3308.
- Wang, Y., Guo, Y., Holguín-Lerma, J.A., Vezzoli, M., and Tang, H.X. (2024, May). Wafer-scale thermal diffusion of titanium into sapphire substrate. In *CLEO: Science and Innovations* (pp. SM1O–1). Optica Publishing Group.

Talks

- **Jane Street:** Asynchronous Accelerator Architecture for Unstructured Sparse Convolutional Neural Networks. May 2025
- **DATE 2024:** Designing an Energy-Efficient Fully-Asynchronous Deep Learning Convolution Engine. March 2024

Extracurricular and Interests

Collaborated with artists from the **Yale School of Art** on the realization of moving sculptures. Designed and implemented the technical components of the projects.

– *Dust Breeder:* Collaboration with Andrew Luk. 2025
– *Inertia:* Collaboration with Rafael Villares. 2023
– *Extra Foot or Two:* Collaboration with Patrick Henry. 2023